



**B.Tech III Semester Supplementary Examinations, July 2022**  
**LOGIC CIRCUITS DESIGN**

(Common to CSE, CSE (AI & ML))

Maximum Marks: 70

Date: 23.07.2022 Duration: 3 hours

- Note: 1. This question paper contains two parts A and B.  
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.  
3. Part B consists of 5 Units. Answer any one full question from each unit.  
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks

(10x2M=20 Marks)

- 1 State De Morgan's theorem?
- 2 Reduce  $A(A + B)$
- 3 Define half adder and full adder
- 4 Define combinational logic?
- 5 Define Flip flop
- 6 Define register and RTL.
- 7 What are the designation of registers?
- 8 What are the Micro operations?
- 9 What is EEPROM?
- 10 What are the Advantages of PAL?

Part-B

Answer All the following questions.

(10M X 5=50Marks)

- 11 (a) Simplify the following expression  $Y = (A + B)(A + C')(B' + C')$ . [5M]  
(b) Convert the octal numbers into binary, decimal, BCD and Hexadecimal numbers (3600)octal, (1200)octal, (0200)octal, (0777)octal [5M]

OR

- 12 a) Simplify the Boolean expressions to minimum number of literals [5M]  
i)  $X' + XY + XZ' + XYZ'$  ii)  $(X+Y)(X+Y')$  [5M]  
b) Obtain the Complement of Boolean Expression  
i)  $A+B+A'B'C$  ii)  $AB + A(B+C) + B'(B+D)$

- 13 (a) Simplify the Boolean expression using K-map [5M]  
 $F(A,B,C,D) = \sum m(0,2,3,7,11,13,14,15)$   
(b) Design a full adder. [5M]

OR

- 14 (a) Explain about binary multiplier and subtracter. [6M]  
(b) Design procedure for combinational circuit with example? [4M]

- 15 (a) Explain detail about JK and D flip-flops. [6M]  
(b) Difference between combinational circuits and sequential circuits [4M]

OR

- 16 (a) Explain about analysis of sequential circuits using D flipflop. [5M]  
(b) Explain shift register and data transfer entering and retrieving methods? [5M]

- 17 (a) Explain Detail about Arithmetic Micro operations? [4M]  
(b) What is Register Transfer Language explain with example? [6M]

OR

- 18 With a neat diagram construct a bus system for 4 registers using multiplexers and also using tri state buffers. [10M]

- 19 (a) A combinational circuit is defined by the functions:  $F_1 = \sum m(3,5,7)$  [4M]  
 $F_2 = \sum m(4,5,7)$  [6M]  
Implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs

(b) With a neat diagram explain in detail about construction of a ROM using decoder.

OR

- 20 (a) Explain about memory Decoding with logical construction of RAM? [4M]  
(b) Implement the following two Boolean function with a PLA

$$F_1(A,B,C) = \sum(0,1,2,4) \quad [6M]$$

$$F_2(A,B,C) = \sum(0,5,6,7)$$